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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,658	02/09/2004	Yoichi Tamaki	XA-10036	7635

181 7590 03/21/2007

MILES & STOCKBRIDGE PC
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EXAMINER	
PHAM, LONG	
ART UNIT	**PAPER NUMBER**
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/773,658	TAMAKI ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 December 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Rejections and/or objections as previously applied

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi et al. (Japan 2002-057219) in combination with Kinoshita (US pat 6,300,669) and Moyer (US patent 5,374,844).

With respect to claims 1, 6, 10, Takashi et al. a semiconductor device comprising (see figs. 1-6 and English abstract):

a) a semiconductor layer 3 that is provided over an insulation layer 2;

b) a plurality of first bipolar transistors 18,19 are provided on the semiconductor layer ; and

c) an first isolation 4-1, 4-4 is provided over a main surface of the semiconductor layer to reach the insulation layer, and provided such that the isolation surrounds a group of or the whole of the plurality of bipolar transistors, such that the surrounded transistors would inherently operate substantially uniformly as constituent elements of a unit transistor.

Takashi et al. fail to teach that the collectors, emitters, and bases of the bipolar transistors are respectively connected in parallel with each other.

Kinoshita teaches collectors, emitters, and bases of a plurality of bipolar transistors are respectively connected in parallel with each other to achieve low-noise, high-power gain high frequency amplifier. See claim 1 and abstract.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Kinoshita into the device of Takashi et al. to attain the above benefit.

With respect to claims 2, 3, 7, 11, and 12, Takashi et al. further fail to teach each of emitter of the plurality of bipolar transistors is connected to a resistor made of polysilicon.

Moyer teaches connecting a polysilicon resistor to an emitter of a bipolar transistor to prevent thermal runaway. See col. 1, lines 35-40.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the teaching of Moyer into the device of Takashi et al. to attain the above benefit.

With respect to claims 4, 5, 8, 9, 13, 14, and 15, Takashi et al. implicitly teach collector and base contact holes but fail to teach the range for the distance between contact holes for the base and collector of plurality of first and second bipolar transistors.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the distance between contact holes for the base and collector through routine experimentation and optimization to obtain optimal or desired device performance because in the absence of unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Further with respect to claim 6, since Takashi et al. in combination with Moyer teach emitters of the bipolar transistors are connected and the emitters are connected to the resistors, the resistors are connected to each other.

Further with respect to claim 10, Takashi et al. further teach a plurality of second bipolar transistors 20, 21 are provided on the semiconductor layer and an second isolation 4-1, 4-4 is provided over a main surface of the semiconductor layer to reach the insulation layer, and provided such that the isolation surrounds a group of or the whole of the plurality of bipolar transistors, such that the

surrounded transistors would inherently operate substantially uniformly as constituent elements of a unit transistor.

Further with respect to claim 10, Takashi et al. in combination with Kinoshita and Moyer further teach that the collectors, emitters, and bases of the bipolar transistors or first and second bipolar transistors are respectively connected in parallel with each other.

With respect to claims 16 and 17, Takashi et al. in combination with Kinoshita and Moyer fail to teach that the optimum current of the first bipolar transistor 1.5 times larger than the second bipolar transistor.

With respect to claim 18, Takashi et al. in combination with Kinoshita and Moyer fail to teach that the relative heat radiation and operation speed of the first bipolar transistor and the second bipolar transistor.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the relative heat radiation and operation speed of the first bipolar transistor and the second bipolar transistor through routine experimentation and optimization to obtain optimal or desired device performance because in the absence of unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Response to Arguments

Applicant's arguments filed 12/19/06 have been fully considered but they are not persuasive. See below.

In response to the applicant's arguments on pages 10 and 11 of the amendment dated 12/19/06, it is submitted that the motivation for incoporating the teaching of Kinoshita into the device of Takashi et al. to achieve low-noise, high-power gain high frequency amplifier.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on Mon-Frid, 10am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Long Pham
Primary Examiner
Art Unit 2814

LP